Remarks

In the Office Action dated May 4, 2006 ("Office Action"), Claims 1-23 and 25-34 were rejected and Claims 24 and 35 were objected to. In the amendment set forth above, Claims 1-4, 6-8, 10, 12, 14, 16, 18-20, 23-26, 28, 30, and 32 were amended and the remaining Claims are as originally presented. In view of this amendment to the Claims and the arguments set forth below, it is submitted that all Claims are in condition for allowance, and a Notice of Allowance is respectfully requested.

1. Amendments to the Specification are provided above as follows:

a.) The paragraph bridging pages 8 and 9 is discussing a very large target memory that may be "on the order of 252 words...". This is a typographical error that should read 2^{52} words, as shown in the correction.

b.) An additional error that appears is several paragraphs of the Specification relates to the way in which a new page address is obtained if a target memory address is not located within any memory look-up table. In particular, if the page address is even, it is obtained from file 114. If the address is odd, the address is obtained from file 115. This is described in Applicants' Specification as follows:

> "The second file 114 is used to page look-up table entry memory spaces, of 051350 words, having even numbered paging addresses and the third file 115 is used to page memory spaces having odd numbered paging addresses." (Specification page 13 lines 9-11.)

Figure 2 shows files 114 and 115 as containing these page addresses.

When the foregoing functionality is being described in regards to Figures 7 and 8, an error was made that describes the page addresses as being obtained from files 112 and 114, rather than from files 114 and 115. This is a typographical error, as may be appreciated from the above-quoted description from page 13 of the Specification. This may further be appreciated upon

considering Figure 2, showing the page addresses as being stored in files 114 and 115.

Replacement paragraphs are provided above to correct this typographical error, and to make these descriptions consistent with the remainder of the Specification.

2. Figures 7 and 8 were corrected to address the problem described in item 1b.) above. That is, the references to "File 1" in steps 196 and 210 were changed to "File 2", and the references to File 2" in those steps were changed to "File 3". This makes these Figures consistent with what is described in the remainder of the Specification and shown in Figure 2. Marked up copies as well as clean copies of these Drawings are submitted herewith.

3. Claims 33 and 34 were rejected under 35 USC §112 as being indefinite for failing to particularly point out the invention because they recite the limitation "said second lookup table" for which there is insufficient antecedent basis. Claim 30 has been amended in the manner suggested by the Examiner to provide this antecedent basis. With this amendment to the Claims, it is believed the Claims satisfy the requirements of 35 USC §112, and this rejection should be withdrawn.

4. Claims 1-23 and 25-34 were rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,530, 823 to Tsuchiya et al. ("Tsuchiya") in view of U.S. Patent No. 6,230,114 to Hellestrand et al. ("Hellestrand"). This rejection is respectfully traversed.

Claim 1 is first considered. As amended, this Claim appears as follows:

1. A main memory simulator for simulating large computer memories, wherein said large computer memories are defined by a plurality of target memory addresses, said simulator comprising:

one or more mass storage devices having page addresses to simulate said target memory addresses;

a memory cache; and

a processor operable with said memory cache, wherein said processor operates under instructions

to move data contained in **a predetermined range of frequently** used target memory addresses between corresponding page addresses in said mass storage devices and said memory cache on a fast memory access basis, and

to move data contained in **a predetermined range of infrequently** used target memory addresses between corresponding page addresses in said mass storage devices and said memory cache on a slow memory access basis.

As may be appreciated from the foregoing, Claim 1, as currently amended, includes several aspects not taught by Tsuchiya or Hellestrand. First, neither reference teaches the aspect of Applicants' invention wherein a memory address is determined to be infrequently used because it is contained in a predetermined range of infrequently used target addresses. Similarly, neither reference teaches that a memory address is determined to be frequently used because it is contained in a range of frequently used addressed.

In addition to the foregoing, Claim 1 has been amended to describe that Applicants' system includes one or more mass storage devices that have page addresses that simulate the target memory addresses of the system that is being simulated. This use of mass storage devices to simulate a target memory system is described throughout Applicants' Specification. (For instance, see the description on pages 7 and 8 of Applicants' Specification in reference to Figures 1 and 2.) Nothing in either Tsuchiya or Hellestrand describe the use of mass storage devices to simulate target memory.

Further to the foregoing point, it may be noted that Tsuchiya is entirely unrelated to simulation at all. Tsuchiya instead describes a table-look-aside buffer for the memory of a computer system. That is, Tsuchiya describes an

actual memory design. Thus, Tsuchiya most certainly does not describe the use of mass storage devices to simulate a target memory.

Hellestrand, unlike Tsuchiya, describes a simulator that is used to simulate processors, not memories. (See Hellestrand Abstract.) Nothing in Hellestrand describes use of mass storage devices to simulate a target memory.

Finally, the combination of Tsuchiya and Hellestrand is improper. Tsuchiya describes an actual memory design. Hellestrand describes a simulator. One skilled in the art would not be motivated to incorporate any of the aspects of a simulator design into an actual memory design for at least the reason that simulation systems are very slow, and are only used as a tool to evaluate the real hardware design. For example, in regards to various simulation techniques including software simulation (ISS) and hardware simulation (e.g., HDL), Hellestrand states:

> "Both the ISS and the architectural hardware model approaches to simulating software are relatively slow, and users of such environments often express frustration at their inability to run simulations at practical speeds. HDL and ISS microprocessor models limit the number of software cycles that can be properly verified on a hardware-software modeling system; a few thousand per second is all they allow. On the other hand, real systems execute 50-1000 million instructions per second or more. From this arises a disparity of a factor between about 10,000 to 200,000 in performance, so that 3 to 60 hours of simulation may be needed to model 1 second of real-time target processor performance." (Hellestrand col. 2 lines 38-49.)

Thus, the disparity in performance between a simulator and the real (target) system that it models is well documented by Hellestrand and others. Since incorporating architectural aspects of a simulator into a target system it models would degrade the performance of the target system, one skilled in the art would not be motivated to make this combination of technologies.

Conversely, one skilled in the art would not be motivated to attempt to incorporate a large-scale virtual memory system of the type taught by Tsuchiya into the simulator of Hellestrand. This is because the Tsuchiya memory has on the order of 2^{53} words of addressed memory (see Tsuchiya Figure 2.) The

Hellestrand simulator does not have enough storage space to simulate this size memory.

For at least the foregoing reasons, one skilled in the art would not be motivated to incorporate aspects of Hellestrand into the system of Tsuchiya or vice versa. This combination of references is therefore improper, and should be withdrawn.

To summarize, neither of the references, alone or in combination, describe one or more storage devices having page addresses to simulate target memory addresses. Moreover, neither of the references, alone or in combination, describes moving data between a page address in mass storage to cache in a manner that is determined based on the range of the target memory in which the data resides. Finally, the combination of references is improper. For all of these reasons, Claim 1 is allowable over this rejection as presently presented.

Claims 2-5 depend from Claim 1 and include additional aspects of the invention not taught or suggested by the cited combination of references. These Claims are allowable for at least the reasons discussed above in regards to Claim 1.

As was the case with Claim 1, independent Claim 6 has been amended to include aspects of Applicants' simulation system within the body of the Claim, rather than reciting those aspects only in the preamble. This Claim has further been amended to describe the aspect wherein the range of target memory addresses in which data is stored determines the memory access scheme used by the simulator to transfer the data. For reasons similar to those described above in regards to Claim 1, Claim 6 is allowable over this rejection, which is improper, and should be withdrawn.

Claims 7-11 depend from Claim 6 and are allowable over this rejection for at least the reasons discussed in Claim 6. These Claims include additional aspects not taught or suggested by the cited combination of references and are allowable over the rejection for additional reasons related to these aspects.

Independent Claims 12, 18, 25 and 30 have been amended in a manner similar to that described above in regards to Claim 1. These Claims are

allowable over this rejection for reasons that are similar to those discussed above in regards to Claim 1.

Dependent Claims 13-17, 19-24, 26-29, and 31-35 depend from a respective one of the base Claims 12, 18, 25, and 30, and are allowable over this rejection for at least the reasons discussed in relation to these base Claims. These Claims include additional aspects not taught or suggested by the cited combination of references and are allowable over the rejection for additional reasons related to these aspects.

5. Claims 24 and 35 were indicated as being allowable if rewritten in independent form. Applicants' appreciate the indication of allowable subject matter in regards to these Claims. It is respectfully submitted that in view of the amendments set forth above, all Claims are now in condition for allowance.

6. The cited references of record that have not been relied upon have been reviewed and are considered to be of general interest only.

Conclusion

In the Office Action dated May 4, 2006, Claims 1-23 and 25-34 were rejected and Claims 24 and 35 were objected to. In the amendment set forth above, Claims 1-4, 6-8, 10, 12, 14, 16, 18-20, 23-26, 28, 30, and 32 were amended and the remaining Claims are as originally presented. In view of this amendment to the Claims and the arguments set forth above, it is respectfully submitted that all Claims are in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner has any questions or concerns, a call to the undersigned is encouraged and appreciated.

Respectfully submitted,

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In re Application of Michael J. Rieschl et al.
Apparatus & Method for the Simulation of a Large Main Memory
dress Space Given Limited Resources
. de #RA 5618 (3203.01US01) - Customer #27516
Attorney: Charles A. Johnson; Reg. #20,852; 651-635-7702
Express Mail ER726458438US
Drawing 7 of 9

Original Showing Markups

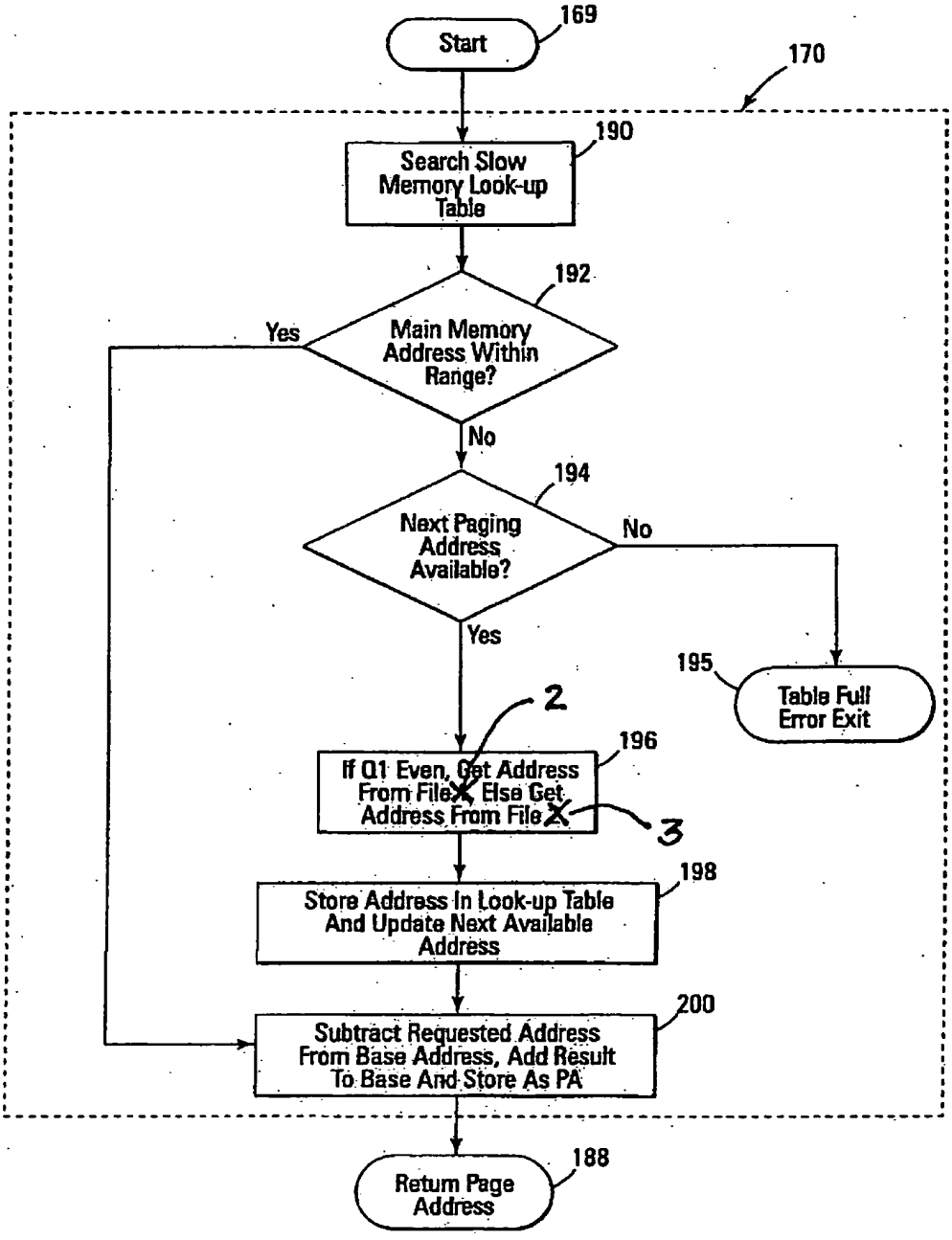

Fig. 7

In re Application of Michael J. Rieschl et al.
Apparatus & Method for the Simulation of a Large Main Memory
Addressing Space Given Limited Resources
File - RA 5618 (3203.01US01) - Customer #27516
Attorney: Charles A. Johnson; Reg. #20,852; 651-635-7702
Express Mail ER726458438US
Drawing8 of 9

Original Showing markups

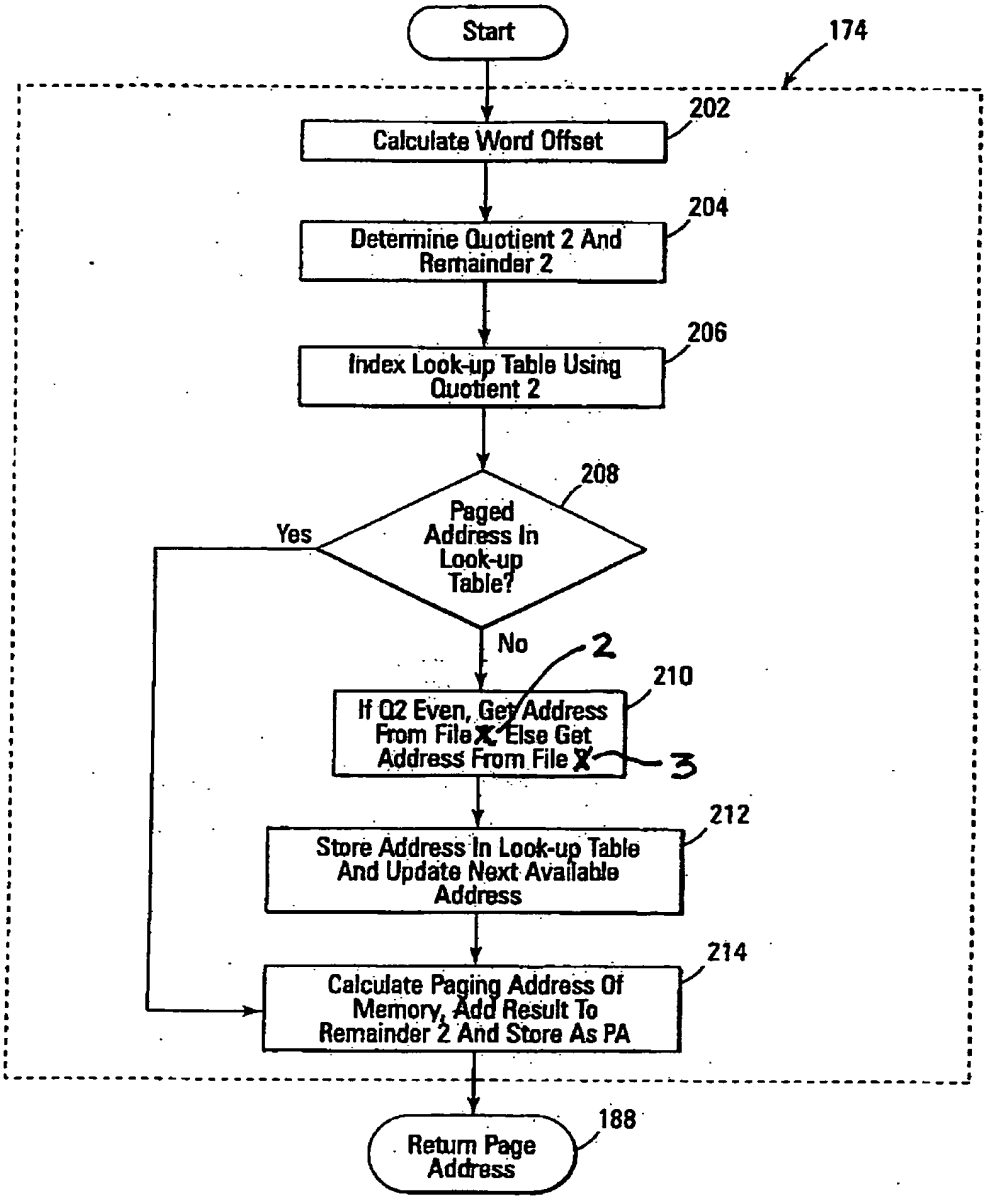

Fig. 8

In re Application of Michael J. Rieschl et al.
Apparatus & Method for the Simulation of a Large Main Memory
Address Space Given Limited Resources
Docket #RA 5618 (3203.01US01) - Customer #27516
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Drawing 7 of 9

Original Showing Markups

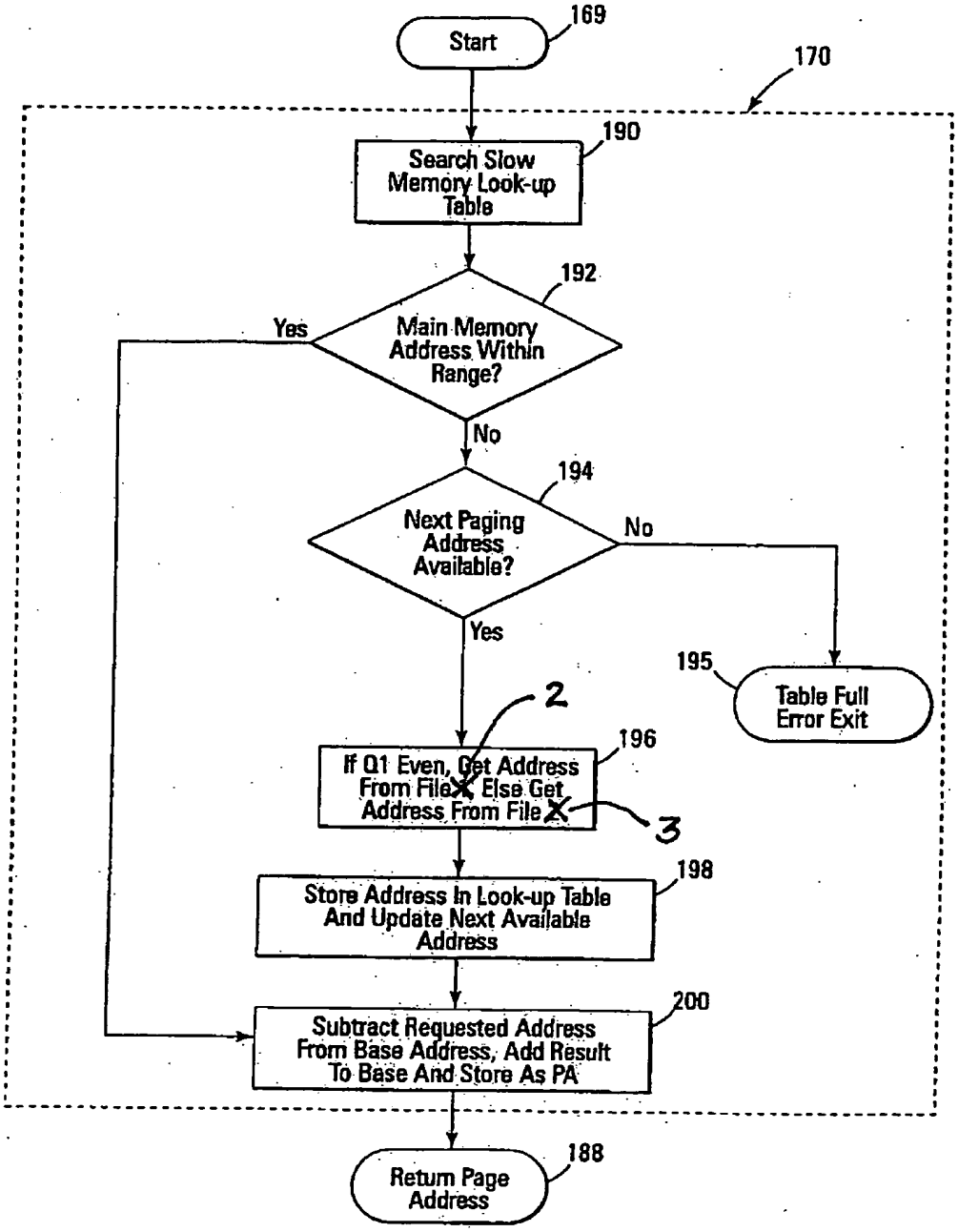

Fig. 7

In re Application of Michael J. Rieschl et al.
Apparatus & Method for the Simulation of a Large Main Memory
Addressing Space Given Limited Resources
File - RA 5618 (3203.01US01) - Customer #27516
Attorney: Charles A. Johnson; Reg. #20,852; 651-635-7702
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Drawing8 of 9

Original Showing markups

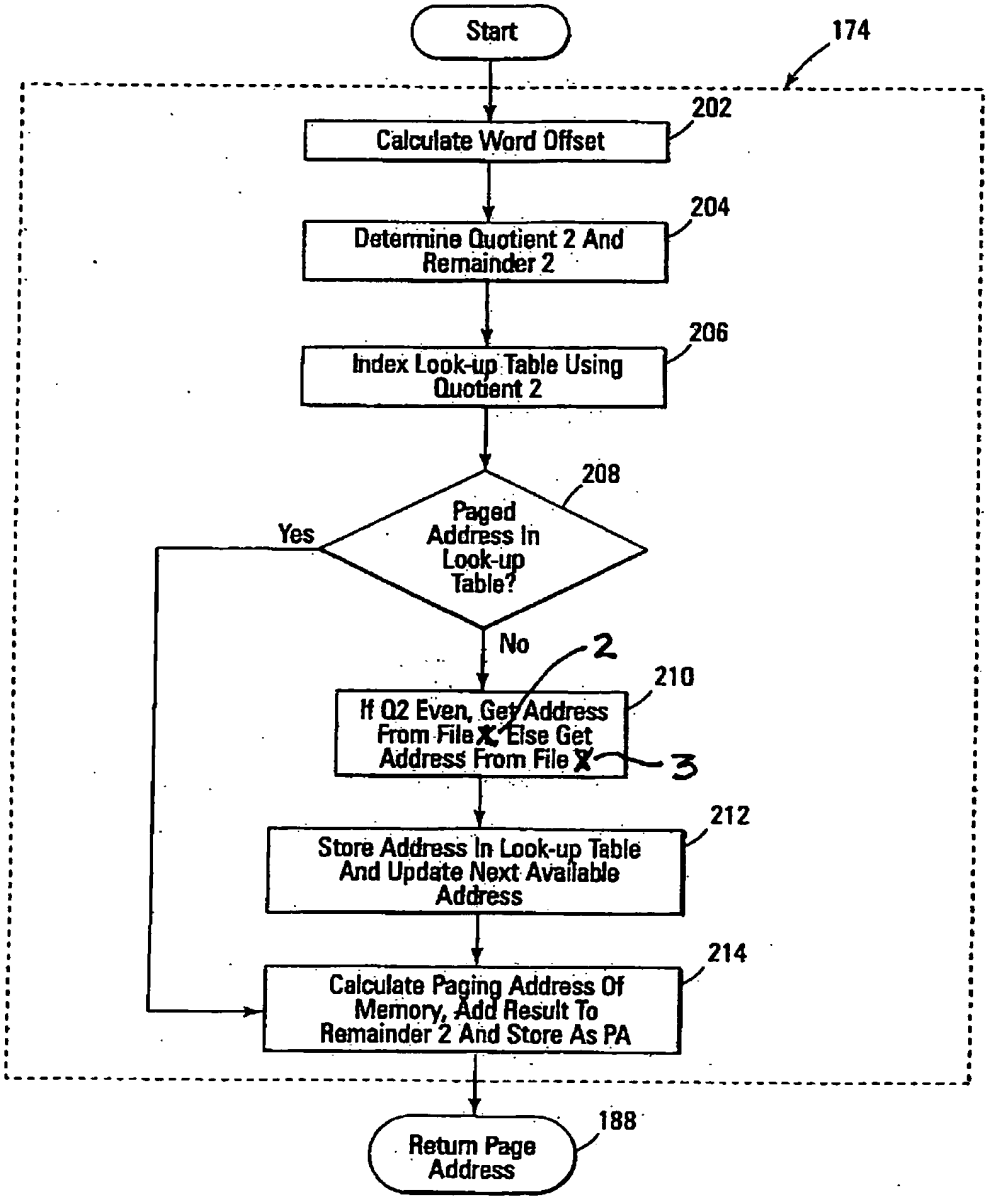

Fig. 8